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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,186	01/22/2004	Hiroshi Nagatomo	OKI.619	2716

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,186	NAGATOMO, HIROSHI	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 6-10* is/are rejected.

7)☒ Claim(s) *2,4,5 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Quek et al. (U.S. 6,417,056).

Regarding claim 1, Quek et al. teaches a method of manufacturing a semiconductor device, comprising the steps of forming a gate electrode on a silicon substrate (column 2, lines 60-65; **20** in Fig. 1); forming first spacers on side surfaces of the gate electrodes, respectively (column 3, lines 4-5; **24** in Fig. 2); chipping off the surface of the silicon substrate with the gate electrode and the first spacers as masks to thereby form steplike portions at positions adjacent to base portions of the first spacers (column 3, lines 39-50; Fig. 7); forming second spacers at the steplike portions respectively (column 3, lines 64-65; **42** in Fig. 10); and forming silicides on the silicon substrate with the first spacers and the second spacers as masks (column 3, line 66 – column 4, line 11; Fig. 11).

Regarding claim 3, Quek et al. teaches the method according to claim 1, and further teaches that the steplike portions are respectively formed to have surfaces vertical to the surface of the silicon substrate (Fig. 8).

Regarding claim 10, Quek et al. teaches the method according to claim 1, and further teaches that the second spacers are formed of an oxide film (column 3, lines 64-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quek et al. (U.S. 6,417,056) in view of Wolf et al. (*Silicon Processing for the VLSI Era*, Vol. 1, second edition, 2000).

Regarding claims 6 and 7, Quek et al. teaches the method according to claim 1 (note 35 U.S.C. 102(b) rejection above), and further teaches that the formation of the silicides is done by depositing a metal on the surface of the silicon substrate and effecting heat treatment thereon, wherein the metal is cobalt (column 4, lines 1-11). Quek et al. is silent, however, regarding the manner in which the cobalt is deposited.

Wolf et al. teaches that sputtering is a commonly accepted method of depositing cobalt for silicide formation, and offers the advantages of films deposited with uniform thickness over large wafers and film thickness control during deposition (pg. 438, section 11.2 and pg. 483, section 11.9).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to manufacture the semiconductor device according to the

method taught by Quek et al. and claim 1, and further form the silicide by depositing cobalt on the surface of the silicon substrate and effecting heat treatment (also taught by Quek et al.), and deposit the cobalt by sputtering, as taught by Wolf et al. The motivation for doing so at the time of the invention would have been because sputtering produces films with uniform thickness over large wafers and offers good film thickness control during deposition, as expressly taught by Wolf et al.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Quek et al. (U.S. 6,417,056) in view of Akasaka et al. (U.S. 6,893,980).

Regarding claim 8, Quek et al. teaches the method according to claim 1 (note 35 U.S.C. 102(b) rejection above), but does not teach that the gate electrode is formed of a polysilicon layer located on a gate oxide film, a tungsten layer located on the polysilicon layer, and a silicon nitride film located on the tungsten layer.

Akasaka et al. teaches a gate electrode formed of a polysilicon layer (**16** in Fig. 4A) located on a gate oxide film (**15** in Fig. 4A), a tungsten layer (**18** in Fig. 4A) located on the polysilicon layer, and a silicon nitride film (**20** in Fig. 4A) located on the tungsten layer (column 8, lines 9-17). The gate electrode formation taught by Akasaka et al. provides a gate electrode wiring that is protected from deterioration (column 2, lines 28-31).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Quek et al. and claim 1, and further form the gate electrode from a polysilicon layer located on a gate oxide film, a tungsten layer located on the polysilicon layer, and a

silicon nitride film located on the tungsten layer, as taught by Akasaka et al. The motivation for doing so at the time of the invention would have been to provide a gate electrode wiring that is protected from deterioration, as expressly taught by Akasaka et al.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Quek et al. (U.S. 6,417,056) in view of Besser et al. (U.S. 6,372,673).

Regarding claim 9, Quek et al. teaches the method according to claim 1 (note 35 U.S.C. 102(b) rejection above). Quek et al. does not teach that a sidewall oxide film is formed on each side surface of the gate electrode and each first spacer is formed thereon.

Besser et al. teaches a method of forming a sidewall oxide film (**7** in Fig. 1) on each side surface of a gate electrode (**2** in Fig. 1) and forming spacers (**8** in Fig. 1) on the oxide film. The oxide film acts as a buffer layer (column 3, lines 16-24).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to manufacture a semiconductor device as taught by Quek et al. and claim 1, and further form an sidewall oxide film on each side surface of the gate electrode and then form spacers on the sidewall oxide film, as taught by Besser et al. The motivation for doing so at the time of the invention would have been to provide a buffer layer, as expressly taught by Besser et al.

Allowable Subject Matter

Claims 2, 4, 5, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art does not teach or suggest, in combination with the other claimed limitations, forming steplike portions that have upward or downward slanting surfaces or curved surfaces convex to the gate electrode.

Prior art also does not teach or suggest, in combination with the other claimed limitations, forming the second spacers by forming an oxide film covering the surface of the silicon substrate and thereafter covering portions of the substrate other than the device region with a resist pattern, and anisotropically etching the oxide film. Quek et al. teaches the opposite approach—forming an oxide film covering the surface of the substrate except the gate electrode, covering the gate electrode and spacer regions with photoresist, and then etching the second sidewall spacers (see Figs. 4-10). There is no motivation to combine this reference with other relevant prior art to arrive at the approach taught in claim 11.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yeap et al. (U.S. 2003/0181028) teaches a method of forming a gate oxide on a silicon substrate, forming first spacers on side surfaces of the gate electrode, forming a recess in the silicon substrate by over-etching during the formation of the first spacers, forming second spacers in the recesses, and forming silicides.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

LAURA M. SCHILLINGER
PRIMARY EXAMINER